In the Claims:

Please amend claims 1, 2, 7-9, 13 and 15, add new claims 17-21, and cancel claims 10-12, 14 and 16 without prejudice or disclaimer as indicated in the following listing of claims, which replaces all prior versions.

1. (Currently amended) A method of compressing data comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits including care bits and don't care bits, the method being characterized by the steps of:

~~(i)~~ comparing corresponding bits of the two or more subsequent vectors to determine if they are compatible; ~~and, if all corresponding bits of said vectors are compatible;~~

~~ii)~~ responsive to determining that all corresponding bits of a number n of said two or more vectors being compatible, merging said ~~two or more~~ n vectors to create a single vector representative thereof; ~~wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values~~ and

reconstructing said n vectors from the merged vector by filling in don't care bits using a selected one of a random fill process and a merge fill process, selection between random fill and merge fill being based on the number n.

2. (Currently amended) A method according to claim 1, wherein said data comprises test vector data for use in testing a logic product, and the method includes ~~the steps of~~ generating or obtaining original test vector data ~~comprising "care" bits and "don't care "bits", and compressing said test vector data according to steps i) and ii)~~.

3. (Original) A method according to claim 2, wherein said original test vector data is generated by means of an Automated Test Pattern Generation (ATPG) tool.

4. (Previously presented) A method according to claim 1, including the step of generating a repeat value in respect of one or more merged vectors, said repeat value being indicative of a number of times the respective merged vector should be repeated to reconstruct the care bits in the vectors of which the merged vector is representative.

5. (Original) A data set comprising test vector data for use in testing a logic product, said test vector data being compressed by the method of claim 4.

6. (Original) A method of testing a logic product, the method comprising the steps of generating compressed test vector data according to claim 5, reconstructing the test vector data by repeating the merged vector one or more times according to their respective repeat values, applying said reconstructed test vector data to an input of said logic product and obtaining the resultant output data.

7. (Currently amended) A method according to claim 6, further comprising the step of compressing said output data comprising a sequence of at least two subsequent output vectors, wherein an output vector comprises one or more bits, the method being characterized by the steps of:

~~(i)~~ comparing corresponding bits of two or more subsequent output vectors to determine if they are compatible; and~~, if all corresponding bits of said vectors are compatible;~~

~~ii)~~ responsive to determining that all corresponding bits of said output vectors are compatible, merging said two or more output vectors to create a single output vector representative thereof~~; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values~~.

8. (Currently amended) Apparatus for compressing data using the method according to claim 1 ~~comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the apparatus being characterized by:~~

~~i) means for comparing corresponding bits of two or more data subsequent vectors to determine if they are compatible; and~~

~~ii) means for merging said two or more vectors in which all corresponding bits of said vectors are compatible, to create a single vector representative of said two or more vectors; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values~~.

9. (Currently amended) Apparatus according to claim 8, wherein said data comprises test vector data for use in testing a logic product~~, and the apparatus includes means for generating or receiving original test vector data comprising a sequence of two or more vectors, wherein a vector comprises one or more bits, including "care" bits and "don't care" bits~~.

10. (Cancelled).

11. (Cancelled).

12. (Cancelled).

13. (Currently amended) Apparatus according to claim 9, including ~~10, wherein said means for generating original test vector data comprises~~ an Automated Test Pattern Generation (ATPG) tool to generate original test vector data.

14. (Cancelled).

15. (Currently amended) Apparatus according to claim 9 ~~10~~, including ~~means for storing~~ a memory to store merged ~~data sequences in the form of a data set~~ vectors for use in testing ~~a~~ the logic product.

16. (Cancelled).

17. (New) A method according to claim 1, wherein the merge fill process proceeds by one or more of repeat fill or repetitive background data fill.

18. (New) A method according to claim 1, wherein the random fill process is used when n is less than a specified number, otherwise the merge fill process is used.

19. (New) A method according to claim 1, wherein the comparing and merging steps are repeated, resulting in a plurality of merged vectors.

20. (New) A method according to claim 19, wherein the merged vectors are arranged in a sequence of merged vector sets, each merged vector set having a first merged vector and a last merged vector, the method further comprising ordering the merged vector sets so that the last merged vector of one merged vector set is compatible with the first merged vector of the subsequent merged vector set.

21. (New) A method according to claim 20, further comprising merging the last merged vector of the one merged vector set with the first merged vector of the subsequent merged vector set.